1. A photosensor for use in an imaging device, said photosensor comprising:

a doped layer of a first conductivity type formed in a substrate;

a first doped region of a second conductivity type formed in said doped layer;

a buried doped region of a second conductivity type formed in said doped layer adjacent said first doped region, wherein said buried doped region is doped at a dopant concentration less that said first doped region; and

a gate formed over said buried doped region for gating an accumulation of charge into said first doped region.

2. The photosensor according to claim 1, wherein said gate is a photogate.

3. The photosensor according to claim 2, further comprising an insulating layer formed between said doped region and said photogate.

4. The photosensor according to claim 3, wherein the insulating layer is a silicon dioxide layer.

5. The photosensor according to claim 3, wherein the insulating layer is a silicon nitride layer.

6. The photosensor according to claim 3, wherein the insulating layer is a layer of ONO.

7. The photosensor according to claim 1, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

8. The photosensor according to claim 1, wherein said first doped region is doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

9. The photosensor according to claim 8, wherein said first doped region is doped with phosphorous.

10. The photosensor according to claim 8, wherein said first doped region is doped at a dopant concentration of from about $1x10^{14}$ ions/cm^2 to about $5x10^{16}$ ions/cm^2.

11. The photosensor according to claim 10, wherein said buried doped region is doped at a dopant concentration of from about $1x10^{11}$ ions/cm^2 to about $1x10^{13}$ ions/cm^2.

12. The photosensor according to claim 1, wherein said buried doped region is doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

13. The photosensor according to claim 12, wherein said buried doped region is doped with phosphorous.

14. The photosensor according to claim 12, wherein said buried doped region is doped at a dopant concentration of from about $1x10^{11}$ ions/cm^2 to about $1x10^{13}$ ions/cm^2.

15. The photosensor according to claim 13, wherein said first doped region is doped at a dopant concentration of from about $1x10^{14}$ ions/cm^2 to about $5x10^{16}$ ions/cm^2.

16. The photosensor according to claim 1, wherein said photosensor is used in a CMOS imager.

17. The photosensor according to claim 2, further comprising a transfer transistor for transferring charge accumulated in said first doped region to a second doped region of said second conductivity type formed in said doped layer of said first conductivity type, wherein the gate of said transfer transistor is formed adjacent said first doped region and over a second buried region of said second conductivity type formed in said doped layer, wherein said second buried doped layer is doped at a dopant concentration less that that of said first and second doped regions.

18. The photosensor according to claim 17, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

19. The photosensor according to claim 17, wherein said first and second doped regions are doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

20. The photosensor according to claim 19, wherein said first and second doped regions are doped with phosphorous.

21. The photosensor according to claim 19, wherein said first and second doped regions are doped at a dopant concentration of from about $1x10^{14}$ ions/cm^2 to about $5x10^{16}$ ions/cm^2.

22. The photosensor according to claim 21, wherein said first and second buried doped regions are doped at a dopant concentration of from about $1x10^{11}$ ions/cm^2 to about $1x10^{13}$ ions/cm^2.

23. The photosensor according to claim 17, wherein said first and second buried doped regions are doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

24. The photosensor according to claim 23, wherein said first and second buried doped regions are doped with phosphorous.

25. The photosensor according to claim 24, wherein said first and second buried doped regions are doped at a dopant concentration of from about $1x10^{11}$ ions/cm^2 to about $1x10^{13}$ ions/cm^2.

26. The photosensor according to claim 24, wherein said first and second doped regions are doped at a dopant concentration of from about $1x10^{14}$ ions/cm^2 to about $5x10^{16}$ ions/cm^2.

27. The photosensor according to claim 17, further comprising a source follower transistor for outputting charge accumulated in said first doped region which has been transferred to said second doped region, wherein the gate of said source follower transistor is formed adjacent said second doped region and over a third buried region of said second conductivity type formed in said doped layer, wherein said third buried doped layer is doped at a dopant concentration less that that of said first and second doped regions.

28. The photosensor according to claim 27, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

29. The photosensor according to claim 27, wherein said first and second doped regions are doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

30. The photosensor according to claim 29, wherein said first and second doped regions are doped with phosphorous.

31. The photosensor according to claim 29, wherein said first and second doped regions are doped at a dopant concentration of from about $1x10^{14}$ ions/cm^2 to about $5x10^{16}$ ions/cm^2.

32. The photosensor according to claim 31, wherein said first, second and third buried doped regions are doped at a dopant concentration of from about $1x10^{11}$ ions/cm^2 to about $1x10^{13}$ ions/cm^2.

33. The photosensor according to claim 27, wherein said first, second and third buried doped regions are doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

34. The photosensor according to claim 33, wherein said first, second and third buried doped regions are doped with phosphorous.

35. The photosensor according to claim 34, wherein said first, second and third buried doped regions are doped at a dopant concentration of from about $1x10^{11}$ ions/cm^2 to about $1x10^{13}$ ions/cm^2.

36. The photosensor according to claim 34, wherein said first and second doped regions are doped at a dopant concentration of from about $1x10^{14}$ ions/cm^2 to about $5x10^{16}$ ions/cm^2.

37. The photosensor according to claim 27, further comprising a reset transistor for resetting said photosensor, wherein the gate of said reset transistor is formed adjacent said second doped region and a third doped region and over a fourth buried region of said second conductivity type formed in said doped layer, wherein said fourth buried doped layer is doped at a dopant concentration less that that of said first and second doped regions.

38. The photosensor according to claim 37, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

39. The photosensor according to claim 37, wherein said first, second and third doped regions are doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

40. The photosensor according to claim 39, wherein said first, second and third doped regions are doped with phosphorous.

41. The photosensor according to claim 39, wherein said first, second and third doped regions are doped at a dopant concentration of from about $1x10^{14}$ ions/cm^2 to about $5x10^{16}$ ions/cm^2.

42. The photosensor according to claim 41, wherein said first, second, third and fourth buried doped regions are doped at a dopant concentration of from about $1x10^{11}$ ions/cm^2 to about $1x10^{13}$ ions/cm^2.

43. The photosensor according to claim 42, wherein said first, second, third and fourth buried doped regions are doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

44. The photosensor according to claim 43, wherein said first, second, third and fourth buried doped regions are doped with phosphorous.

45. The photosensor according to claim 44, wherein said first, second, third and fourth buried doped regions are doped at a dopant concentration of from about $1x10^{11}$ ions/cm^2 to about $1x10^{13}$ ions/cm^2.

46. The photosensor according to claim 44, wherein said first, second and third doped regions are doped at a dopant concentration of from about $1x10^{14}$ ions/cm^2 to about $5x10^{16}$ ions/cm^2.

47. An imaging device comprising:

a doped layer of a first conductivity type formed in a substrate;

a first doped region of a second conductivity type formed in said doped layer, said first doped region forming a charge collection area in said imaging device;

a second doped region of said second conductivity type formed in said doped layer, said second doped region forming a diffusion region in said imaging device for receiving charge from said charge collection region;

a buried doped region of said second conductivity type formed in said doped layer adjacent said second doped region, wherein said buried doped region is doped at a dopant concentration less that said first doped region; and

a source follower transistor connected to said second doped region and wherein the gate of said source follower transistor is formed over said buried doped region.

48. The imaging device according to claim 47, further comprising an insulating layer formed between said first doped region and said gate.

49. The imaging device according to claim 48, wherein the insulating layer is a silicon dioxide layer.

50. The imaging device according to claim 48, wherein the insulating layer is a silicon nitride layer.

51. The imaging device according to claim 48, wherein the insulating layer is a layer of ONO.

52. The imaging device according to claim 47, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

53. The imaging device according to claim 47, wherein said first and second doped regions are doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

54. The imaging device according to claim 53, wherein said first and second doped regions are doped with phosphorous.

55. The imaging device according to claim 53, wherein said first and second doped regions are doped at a dopant concentration of from about $1x10^{14}$ ions/cm^2 to about $5x10^{16}$ ions/cm^2.

56. The imaging device according to claim 53, wherein said buried doped region is doped at a dopant concentration of from about $1x10^{11}$ ions/cm^2 to about $1x10^{13}$ ions/cm^2.

57. The imaging device according to claim 47, wherein said buried doped region is doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

58. The imaging device according to claim 57, wherein said buried doped region is doped with phosphorous.

59. The imaging device according to claim 57, wherein said buried doped region is doped at a dopant concentration of from about $1x10^{11}$ ions/cm^2 to about $1x10^{13}$ ions/cm^2.

60. The imaging device according to claim 58, wherein said buried doped region is doped at a dopant concentration of from about $1x10^{11}$ ions/cm^2 to about $1x10^{13}$ ions/cm^2.

61. A photosensor for use in an imaging device, comprising:

a doped layer of a first conductivity type formed in a substrate;

a first doped region of a second conductivity type formed in said doped layer;

a first buried doped region of said second conductivity type formed in said doped layer adjacent said first doped region, wherein said first buried doped region is doped at a dopant concentration less that of said first doped region;

a photogate over said buried doped region for gating the accumulation of charge stored into said first doped region;

a second doped region formed in said doped layer spaced from said first doped region for receiving charge transferred from said first doped region;

a second buried doped region of said second conductivity type formed in said doped layer adjacent said first doped region and said second doped region, wherein said second buried doped region is doped at a dopant concentration less that said first and second doped regions;

a transfer gate over said second buried doped region for transferring charge accumulated in said first doped region to said second doped region;

a reset transistor for periodically resetting said second doped region to a predetermined potential; and

an output transistor having a gate connected to said second doped region for providing a signal representing image charge transferred to said second doped region.

62. The photosensor according to claim 61, further comprising an insulating layer formed over said first and second doped regions and underneath said photogate and said transfer device.

63. The photosensor according to claim 62, wherein the insulating layer is a silicon dioxide layer.

64. The photosensor according to claim 62, wherein the insulating layer is a silicon nitride layer.

65. The photosensor according to claim 62, wherein the insulating layer is a layer of ONO.

66. The photosensor according to claim 61, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

67. The photosensor according to claim 61, wherein said first doped region and said second doped region are doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

68. The photosensor according to claim 67, wherein said first doped region and said second doped region are doped with phosphorous.

69. The photosensor according to claim 67, wherein said first doped region and said second doped region are doped at a dopant concentration of from about $1x10^{14}$ ions/cm^2 to about $5x10^{16}$ ions/cm^2.

70. The photosensor according to claim 69, wherein said first and second buried doped regions are doped at a dopant concentration of from about $1x10^{11}$ ions/cm^2 to about $1x10^{13}$ ions/cm^2.

71. The photosensor according to claim 61, wherein said first and second buried doped regions are doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

72. The photosensor according to claim 71, wherein said first and second buried doped regions are doped with phosphorous.

73. The photosensor according to claim 71, wherein said first and second buried doped regions are doped at a dopant concentration of from about $1x10^{11}$ ions/cm^2 to about $1x10^{13}$ ions/cm^2.

74. The photosensor according to claim 73, wherein said first doped region and said second doped region are doped at a dopant concentration of from about $1x10^{14}$ ions/cm^2 to about $5x10^{16}$ ions/cm^2.

75. A CMOS imager system comprising:

(i) a processor; and

(ii) a CMOS imaging device coupled to said processor, said CMOS imaging system comprising:

a doped layer of a first conductivity type formed in a substrate;

a first doped region of a second conductivity type formed in said doped layer;

a buried doped region of a second conductivity type formed in said doped layer adjacent said first doped region, wherein said buried doped region is doped at a dopant concentration less that said first doped region; and

a photogate over said buried doped region for gating the accumulation of charge into said first doped region.

76. The system according to claim 75, further comprising an insulating layer formed between said doped region and said photogate.

77. The system according to claim 76, wherein the insulating layer is a silicon dioxide layer.

78. The system according to claim 76, wherein the insulating layer is a silicon nitride layer.

79. The system according to claim 76, wherein the insulating layer is a layer of ONO.

80. The system according to claim 75, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

81. The system according to claim 75, wherein said first doped region is doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

82. The system according to claim 81, wherein said first doped region is doped with phosphorous.

83. The system according to claim 81, wherein said first doped region is doped at a dopant concentration of from about $1x10^{14}$ ions/cm^2 to about $5x10^{16}$ ions/cm^2.

84. The system according to claim 83, wherein said buried doped region is doped at a dopant concentration of from about $1x10^{11}$ ions/cm^2 to about $1x10^{13}$ ions/cm^2.

85. The system according to claim 75, wherein said buried doped region is doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

86. The system according to claim 75, wherein said buried doped region is doped with phosphorous.

87. The system according to claim 85, wherein said buried doped region is doped at a dopant concentration of from about $1x10^{11}$ ions/cm^2 to about $1x10^{13}$ ions/cm^2.

88. A CMOS imager system comprising:

(i) a processor; and

(ii) a CMOS imaging device coupled to said processor, said CMOS imaging system comprising:

a doped layer of a first conductivity type formed in a substrate;

a first doped region of a second conductivity type formed in said doped layer, said first doped region forming a photocollection area in said imaging device;

a second doped region of a second conductivity type formed in said doped layer, said second doped layer forming a diffusion region in said imaging device;

a buried doped region of a second conductivity type formed in said doped layer adjacent said second doped region, wherein said buried doped region is doped at a dopant concentration less that said first doped region; and

a source follower transistor connected to said second doped region and wherein the gate of said source follower transistor is formed over said buried doped region.

89. The system according to claim 88, further comprising an insulating layer formed between said doped region and said gate.

90. The system according to claim 89, wherein the insulating layer is a silicon dioxide layer.

91. The system according to claim 89, wherein the insulating layer is a silicon nitride layer.

92. The system according to claim 89, wherein the insulating layer is a layer of ONO.

93. The system according to claim 88, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

94. The system according to claim 88, wherein said first and second doped regions are doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

95. The system according to claim 94, wherein said first doped region is doped with phosphorous.

96. The system according to claim 94, wherein said first and second doped regions are doped at a dopant concentration of from about $1x10^{14}$ ions/cm^2 to about $5x10^{16}$ ions/cm^2.

97. The system according to claim 96, wherein said buried doped region is doped at a dopant concentration of from about $1x10^{11}$ ions/cm^2 to about $1x10^{13}$ ions/cm^2.

98. The system according to claim 88, wherein said buried doped region is doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

99. The system according to claim 88, wherein said buried doped region is doped with phosphorous.

100. The system according to claim 98, wherein said buried doped region is doped at a dopant concentration of from about $1x10^{11}$ ions/cm^2 to about $1x10^{13}$ ions/cm^2.

101. The system according to claim 100, wherein said first and second doped regions are doped at a dopant concentration of from about $1x10^{14}$ ions/cm^2 to about $5x10^{16}$ ions/cm^2.

102. The system according to claim 88, wherein said first doped region is doped at a dopant concentration of from about $1x10^{14}$ ions/cm^2 to about $5x10^{16}$ ions/cm^2.

103. A CMOS imager system comprising:

(i) a processor; and

(ii) a CMOS imaging device coupled to said processor, said CMOS imaging system comprising:

a doped layer of a first conductivity type formed in a substrate;

a first doped region of a second conductivity type formed in said doped layer;

a first buried doped region of a second conductivity type formed in said doped layer adjacent said first doped region, wherein said first buried doped region is doped at a dopant concentration less that said first doped region;

a photogate over said buried doped region for gating the accumulation of charge into said first doped region;

a second doped region formed in said doped layer spaced from said first doped region for receiving image charge transferred from said first doped region;

a second buried doped region of a second conductivity type formed in said doped layer adjacent said first doped region and said second doped region, wherein said second buried doped region is doped at a dopant concentration less that said first and second doped regions;

a transfer gate over said second buried doped region for transferring charge accumulated in said first doped region;

a reset transistor for periodically resetting said second doped region to a predetermined potential; and

an output transistor having a gate connected to said second doped region for providing a signal representing image charge transferred to said second doped region.

104. The system according to claim 103, further comprising an insulating layer formed between said first and second doped regions and said photogate and said transfer device.

105. The system according to claim 104, wherein the insulating layer is a silicon dioxide layer.

106. The system according to claim 104, wherein the insulating layer is a silicon nitride layer.

107. The system according to claim 104, wherein the insulating layer is a layer of ONO.

108. The system according to claim 103, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

109. The system according to claim 103, wherein said first doped region and said second doped region are doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

110. The system according to claim 109, wherein said first doped region and said second doped region are doped with phosphorous.

111. The system according to claim 109, wherein said first doped region and said second doped region are doped at a dopant concentration of from about $1x10^{14}$ ions/cm^2 to about $5x10^{16}$ ions/cm^2.

112. The system according to claim 111, wherein said first and second buried doped regions are doped at a dopant concentration of from about $1x10^{11}$ ions/cm^2 to about $1x10^{13}$ ions/cm^2.

113. The system according to claim 103, wherein said first and second buried doped regions are doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

114. The system according to claim 113, wherein said first and second buried doped regions are doped with phosphorous.

115. The system according to claim 113, wherein said first and second buried doped regions are doped at a dopant concentration of from about $1x10^{11}$ ions/cm^2 to about $1x10^{13}$ ions/cm^2.

116. The system according to claim 113, wherein said first doped region and said second doped region are doped at a dopant concentration of from about $1x10^{14}$ ions/cm^2 to about $5x10^{16}$ ions/cm^2.

117. The system according to claim 103, wherein said system is a camera system.

118. The system according to claim 103, wherein said system is a scanner.

119. The system according to claim 103, wherein said system is a machine vision system.

120. The system according to claim 103, wherein said system is a vehicle navigation system.

121. The system according to claim 103, wherein said system is a video telephone system.

122. An integrated circuit imager comprising:

an array of pixel sensor cells formed in a substrate, each pixel sensor cell comprising at least one gating device, including a gate, for transferring charge within the cell and a buried doped region formed beneath said gating of employed sensor cell;

signal processing circuitry formed in said substrate and electrically connected to the array for receiving and processing signals representing an image output by the array and for providing output data representing said image; and

a processor for receiving and processing said output data representing said image.

123. An integrated circuit CMOS imager comprising:

an array of pixel sensor cells formed in a doped layer of a substrate, each of said cells comprising:

a first doped region for accumulating image charge;

a second doped region for receiving and outputting image charge received from said first doped region;

a third doped region in said substrate formed at least between first and second doped regions;

signal processing circuitry electrically connected to the array for receiving image charge from the second doped regions and the array and for providing output data representing an image; and

a processor for receiving and processing said output data representing said image.

124. A method of forming a CMOS imager substrate having improved surface charge loss properties, comprising the steps of:

providing a semiconductor substrate having a doped layer of a first conductivity type; and

forming a shallow contiguous buried doped region of a second conductivity type beneath the entire surface of said semiconductor substrate.

125. The method according to claim 124, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

126. The method according to claim 124, wherein the semiconductor substrate is a silicon substrate.

127. The method according to claim 124, wherein the doping step comprises ion implantation.

128. The method according to claim 124, wherein said buried doped region is doped with a dopant selected from the group consisting of arsenic, antimony and phosphorous.

129. The method according to claim 128, wherein said buried doped region is doped at a dopant concentration of from about $1x10^{11}$ ions/cm^2 to about $1x10^{13}$ ions/cm^2.

130. The method according to claim 129, wherein said doped layer is doped at a dopant concentration of from about $1x10^{14}$ ions/cm^2 to about $5x10^{16}$ ions/cm^2.

131. A method of forming an imaging device, comprising the steps of:

providing a semiconductor substrate having a doped layer of a first conductivity type;

forming a first doped region of a second conductivity type in the doped layer;

forming a second doped region of said second conductivity type in the doped layer spaced from said first doped region;

forming a third doped region of said second conductivity type in the doped layer spaced from said second doped region;

forming a buried doped region of said second conductivity type in said doped layer adjacent said first and second doped regions and adjacent said second and third doped regions, wherein said buried doped region is doped at a dopant concentration less than said first, second and third doped regions;

forming a photogate over said buried doped region adjacent said first doped region;

forming a transfer gate over said buried doped region between said second and said third doped regions;

forming a contact between said second doped region and a source follower transistor wherein the gate of said source follower transistor is formed over said buried doped region.

132. The method according to claim 131, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

133. The method according to claim 131, wherein said first doped region, said second doped region and said third doped region are formed by ion implantation.

134. The method according to claim 133, wherein said first doped region, said second doped region and said third doped region are doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

135. The method according to claim 134, wherein the dopant is phosphorus.

136. The method according to claim 134, wherein said first doped region, said second doped region and said third doped region are doped at a dopant concentration of from about $1x10^{14}$ ions/cm^2 to about $5x10^{16}$ ions/cm^2.

137. The method according to claim 131, wherein said buried doped region is formed by ion implantation.

138. The method according to claim 131, wherein said buried doped region is formed under the entire surface of said doped layer.

139. The method according to claim 131, wherein said buried doped region is doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

140. The method according to claim 139, wherein said dopant is phosphorous.

141. The method according to claim 139, wherein said buried doped region is doped at a dopant concentration of from about $1x10^{11}$ ions/cm^2 to about $1x10^{13}$ ions/cm^2.

142. A method of forming an imaging device, comprising the steps of:

providing a semiconductor substrate having a doped layer of a first conductivity type;

forming a first doped region of a second conductivity type in the doped layer;

forming a second doped region of said second conductivity type in the doped layer spaced from said first doped region;

forming a third doped region of said second conductivity type in the doped layer spaced from said second doped region;

forming a photogate over said first doped region;

forming a transfer gate over said second and said third doped regions;

forming a contact between said second doped region and a source follower transistor wherein the gate of said source follower transistor is over said substrate;

forming a buried doped region of said second conductivity type in said doped layer adjacent said first and second doped regions and adjacent said second and third doped regions and under said photogate, transfer gate and said source follower transistor gate, wherein said buried doped region is doped at a dopant concentration less than said first, second and third doped regions.

143. The method according to claim 142, wherein the first conductivity type is p-type, and the second conductivity type is n-type.

144. The method according to claim 142, wherein said first doped region, said second doped region and said third doped region are formed by ion implantation.

145. The method according to claim 144, wherein said first doped region, said second doped region and said third doped region are doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

146. The method according to claim 145, wherein the dopant is phosphorus.

147. The method according to claim 145, wherein said first doped region, said second doped region and said third doped region are doped at a dopant concentration of from about $1x10^{14}$ ions/cm^2 to about $5x10^{16}$ ions/cm^2.

148. The method according to claim 142, wherein said buried doped region is formed by ion implantation.

149. The method according to claim 142, wherein said buried doped region is formed under the entire surface of said doped layer.

150. The method according to claim 142, wherein said buried doped region is doped with dopants selected from the group consisting of arsenic, antimony and phosphorous.

151. The method according to claim 150, wherein said dopant is phosphorous.

152. The method according to claim 150, wherein said buried doped region is doped at a dopant concentration of from about $1x10^{11}$ ions/cm^2 to about $1x10^{13}$ ions/cm^2.